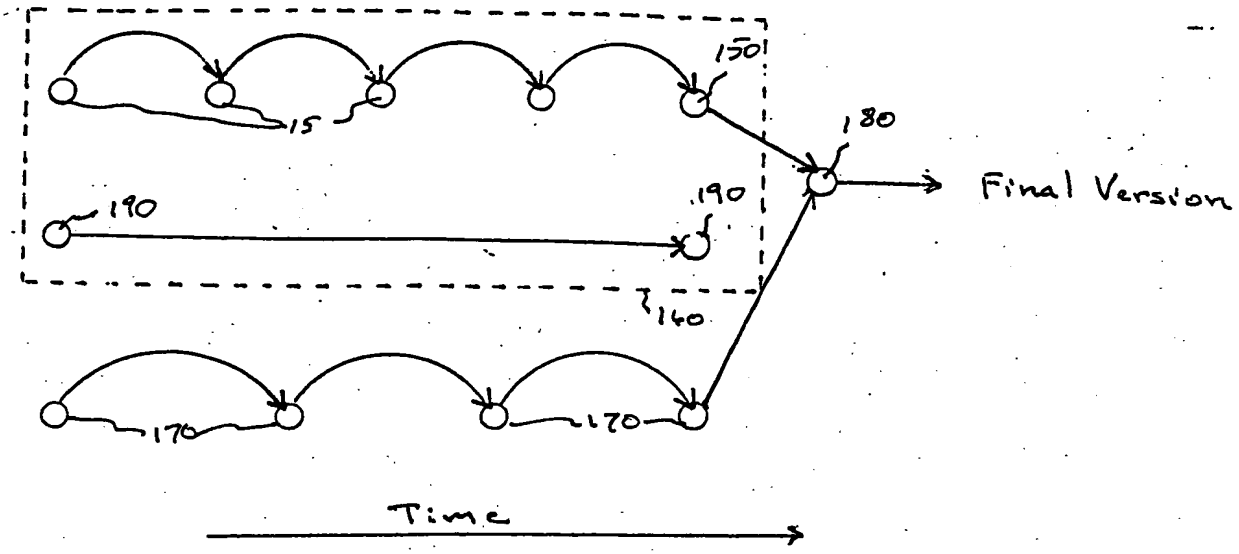

150
15
180
Final Version
190
190
140
170
170
Time

Fig. 1.

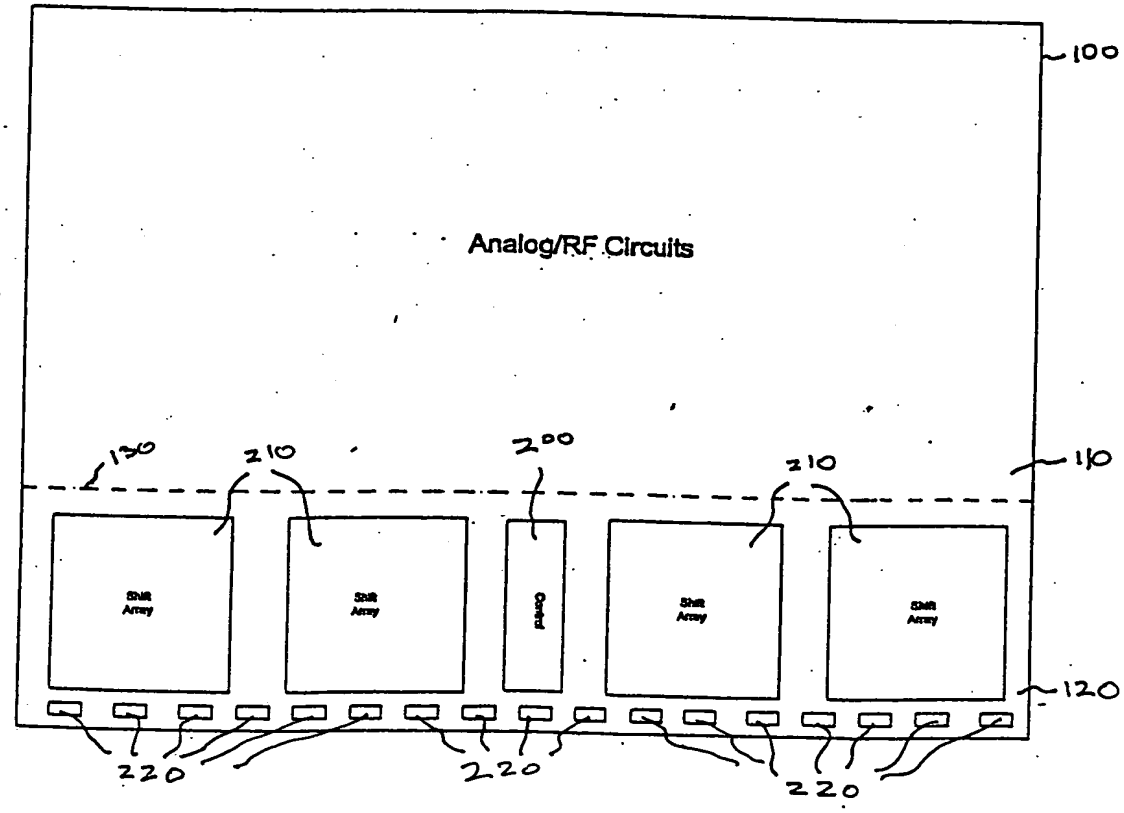

100
Analog/RF Circuits
130
210
200
210
110
Shift Array
Shift Array
Shift Array
Shift Array
120
220
220
220

Fig. 2

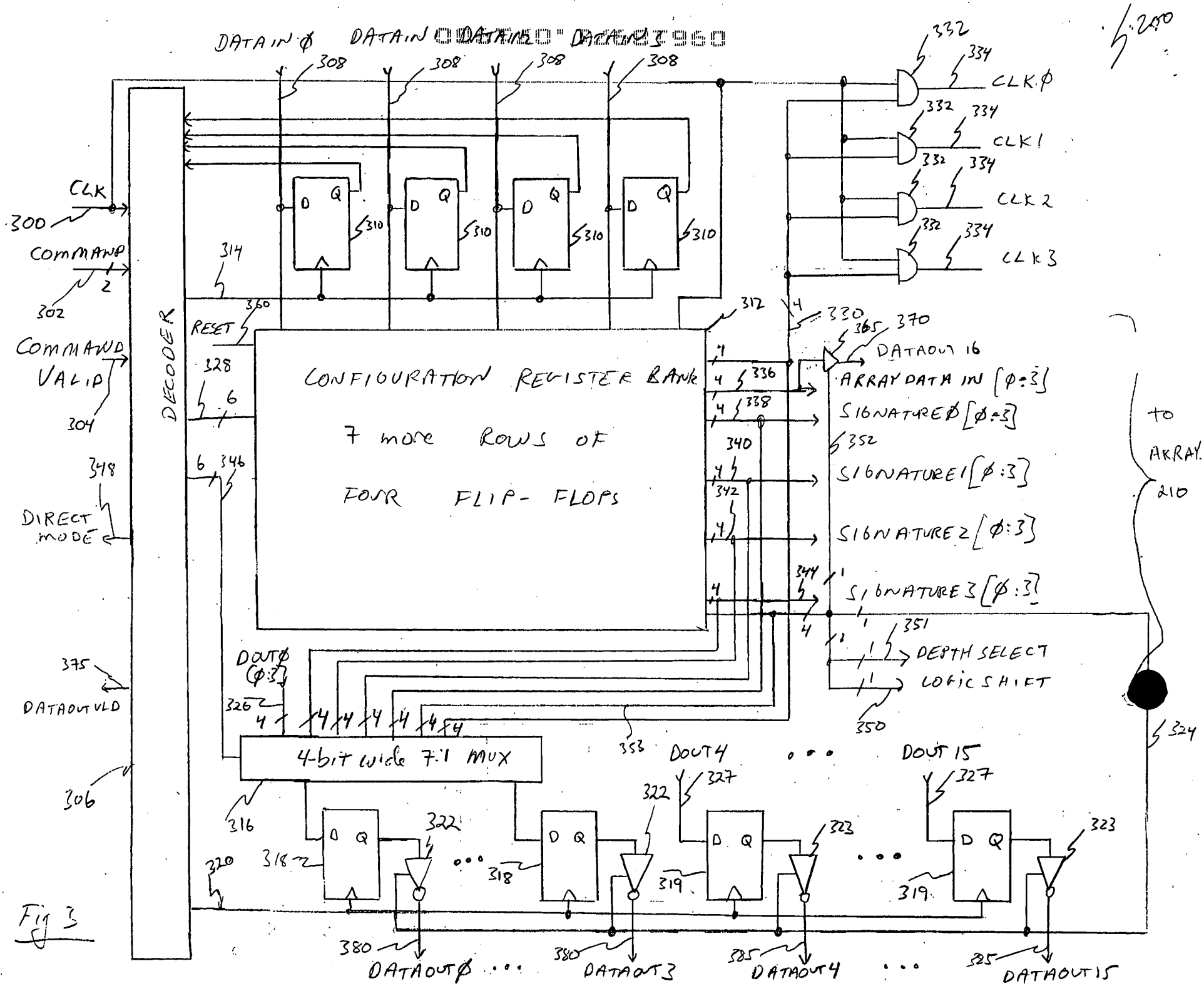
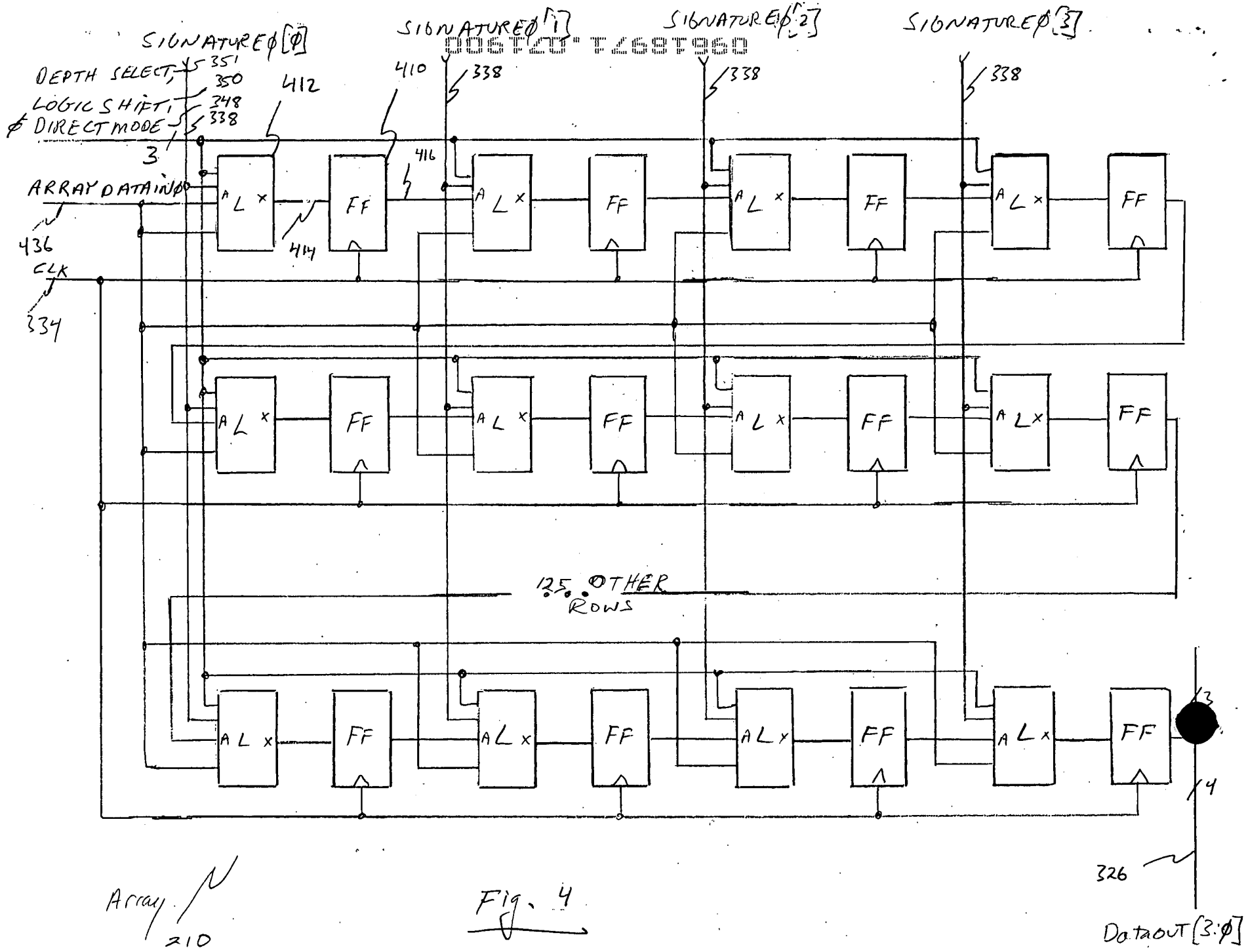

DATA IN Ø
DATA IN 1
DATA IN 2
DATA IN 3
308
CLK
300
COMMAND
2
302
COMMAND VALID
304
DIRECT MODE
348
DECODER
306
DATAOUT VLD
375
RESET
360
314
328
6
346
CONFIGURATION REGISTER BANK
7 more ROWS OF
FOUR FLIP-FLOPS
312
330
332
334
CLK Ø
CLK 1
CLK 2
CLK 3
365
370
DATAOUT 16
ARRAY DATA IN [Ø:3]
SIGNATURE Ø [Ø:3]
SIGNATURE 1 [Ø:3]
SIGNATURE 2 [Ø:3]
SIGNATURE 3 [Ø:3]
336
338
340
342
344
352
351
DEPTH SELECT
LOGIC SHIFT
350
to ARRAY
210
324
DOUTØ [Ø:3]
326
4-bit wide 7:1 MUX
316
353
DOUT4
DOUT15
322
327
323
318
319
320
380
DATAOUTØ
DATAOUT3
385
DATAOUT4
DATAOUT15

Fig 3




Array 210

Fig. 4

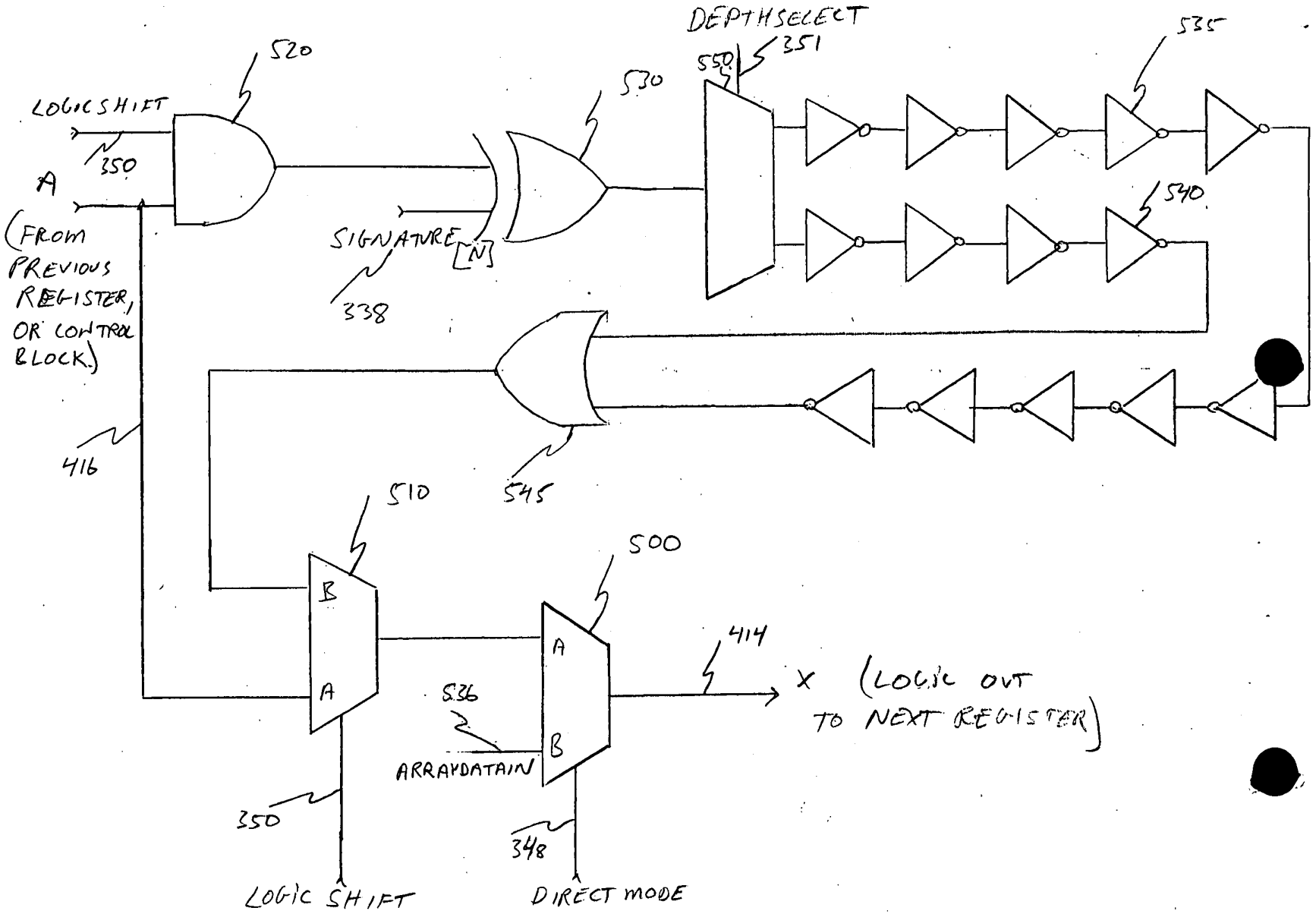

DEPTH SELECT
351
520
530
535
550
LOGIC SHIFT
350
A
(FROM PREVIOUS REGISTER, OR CONTROL BLOCK)
SIGNATURE [N]
338
540
416
545
510
500
B
A
A
B
414
X (LOGIC OUT TO NEXT REGISTER)
536
ARRAYDATAIN
350
348
LOGIC SHIFT
DIRECT MODE

Fig. 5.

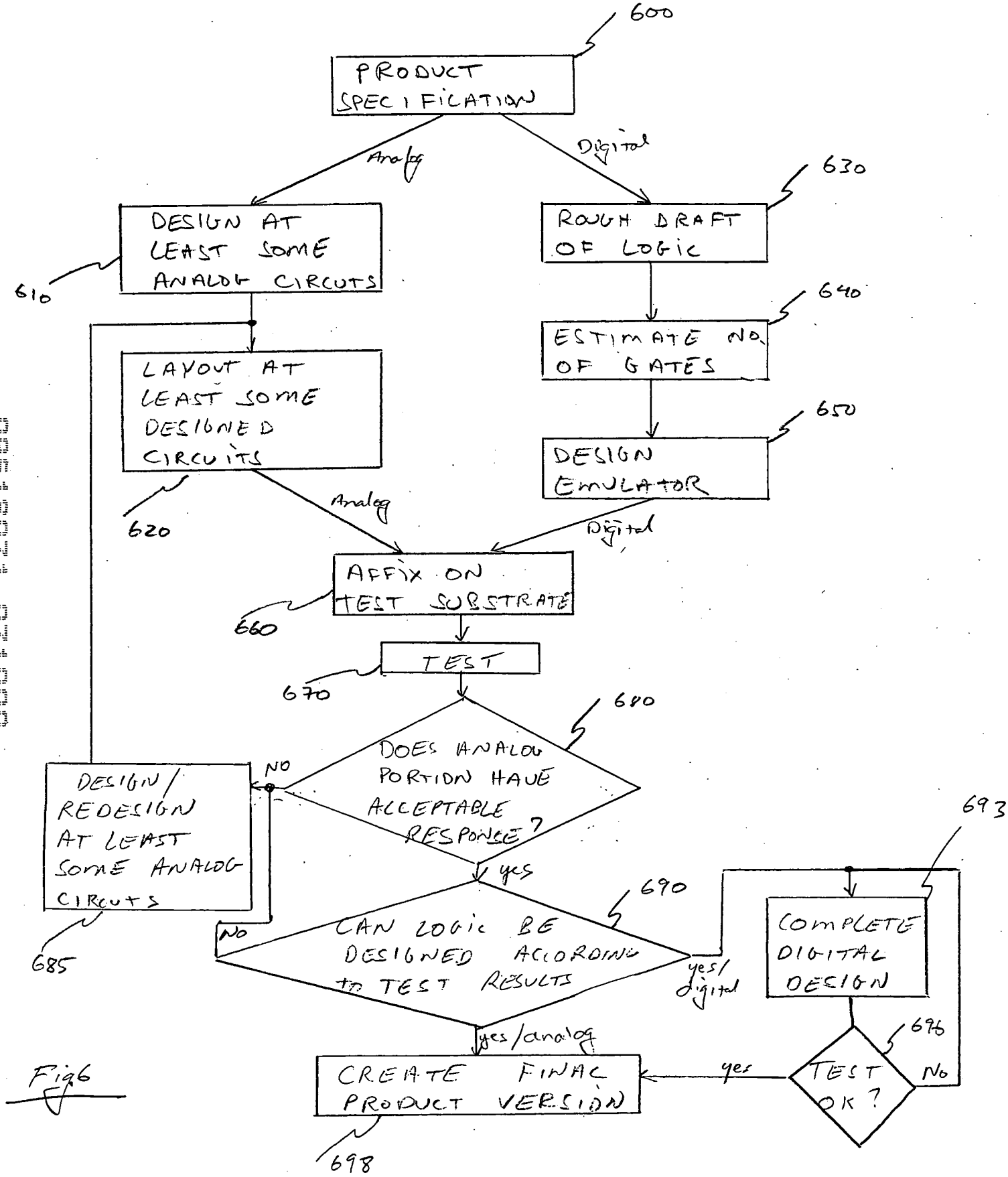

600
PRODUCT SPECIFICATION
Analog
Digital
630
DESIGN AT LEAST SOME ANALOG CIRCUITS
610
ROUGH DRAFT OF LOGIC
640
ESTIMATE NO. OF GATES
650
LAYOUT AT LEAST SOME DESIGNED CIRCUITS
620
DESIGN EMULATOR
Analog
Digital
AFFIX ON TEST SUBSTRATE
660
TEST
670
680
DOES ANALOG PORTION HAVE ACCEPTABLE RESPONSE?
NO
DESIGN/ REDESIGN AT LEAST SOME ANALOG CIRCUITS
685
yes
690
CAN LOGIC BE DESIGNED ACCORDING TO TEST RESULTS
No
yes/digital
693
COMPLETE DIGITAL DESIGN
696
TEST OK?
yes
No
yes/analog
CREATE FINAL PRODUCT VERSION
698

Fig 6

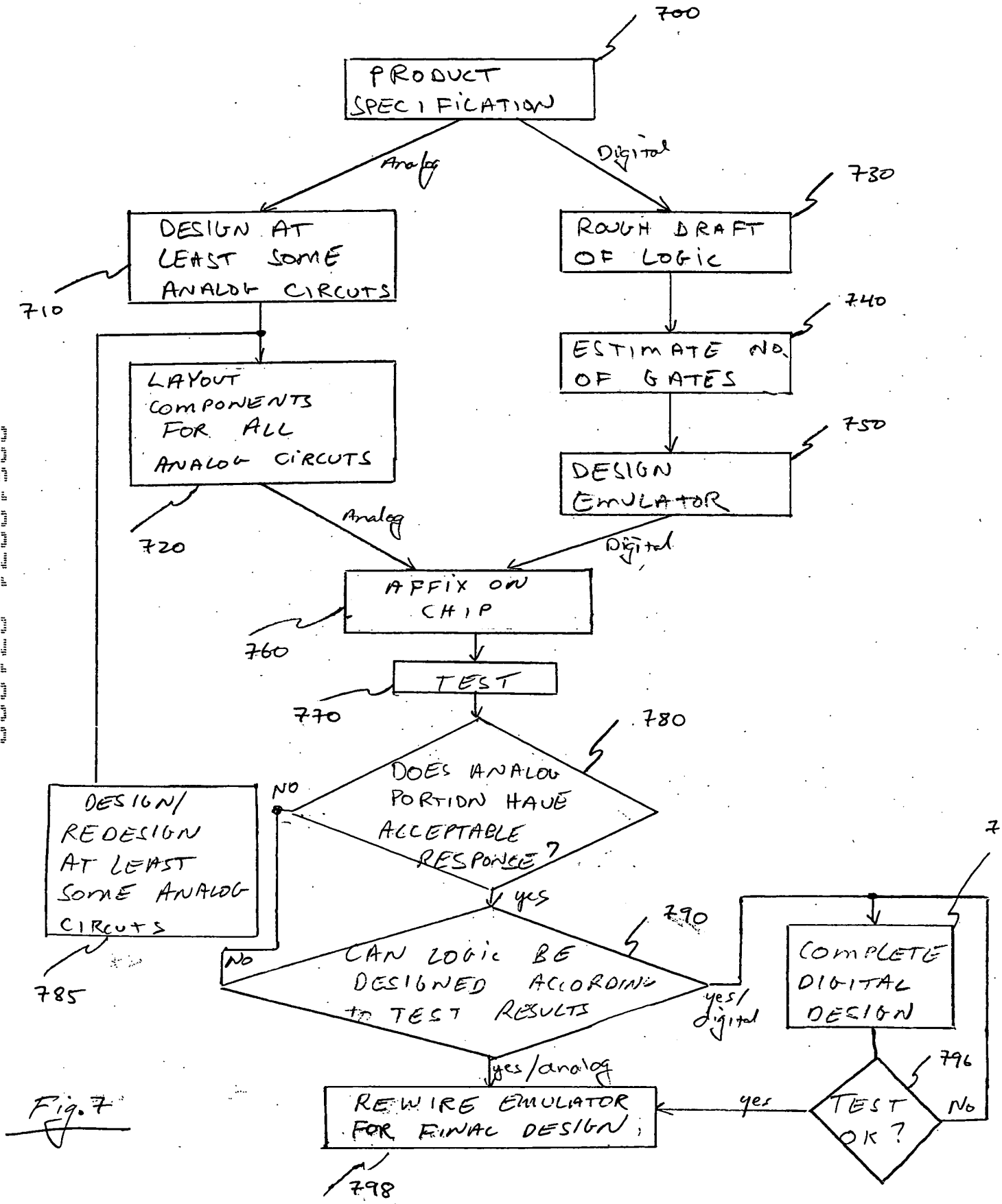
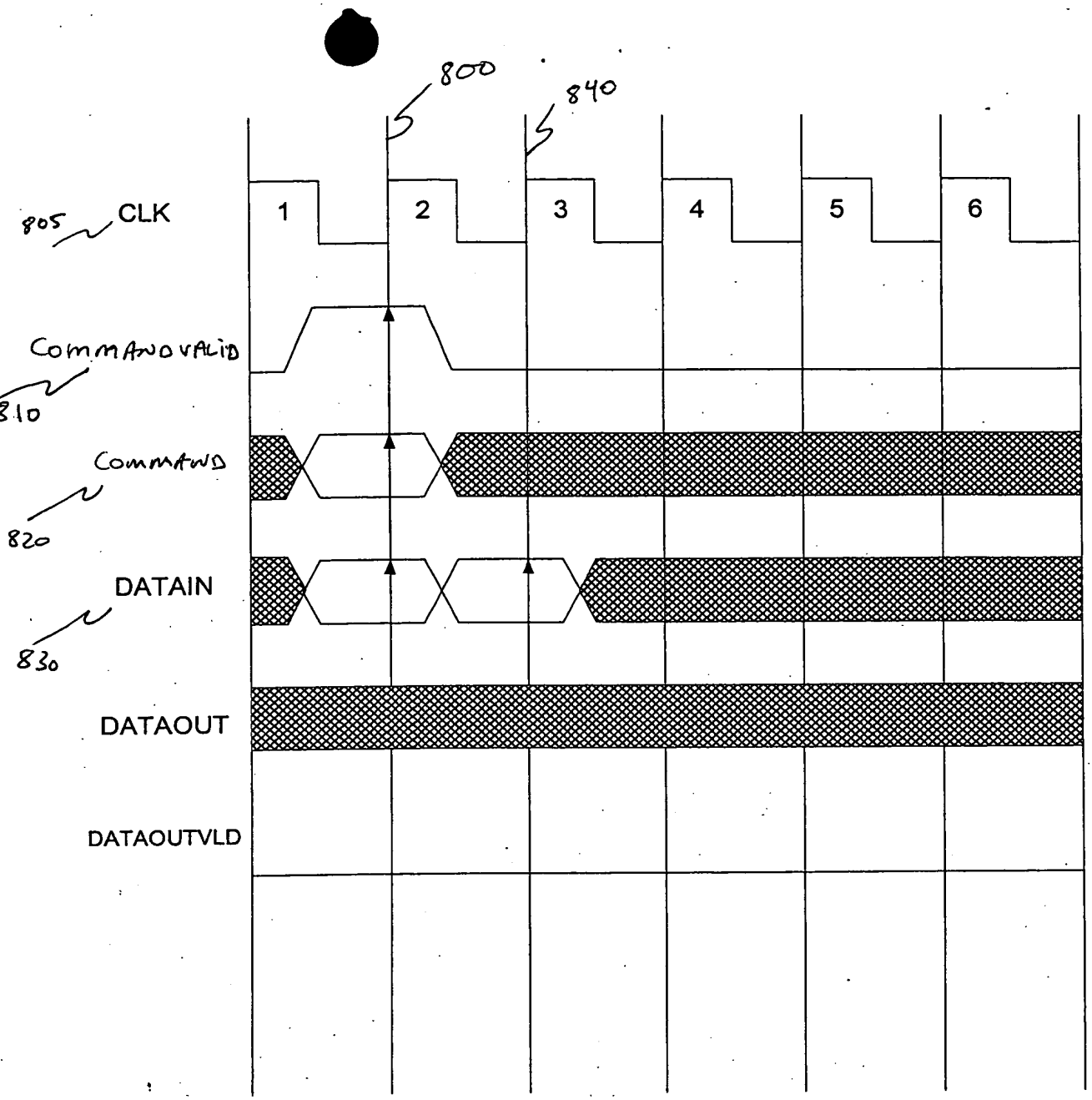
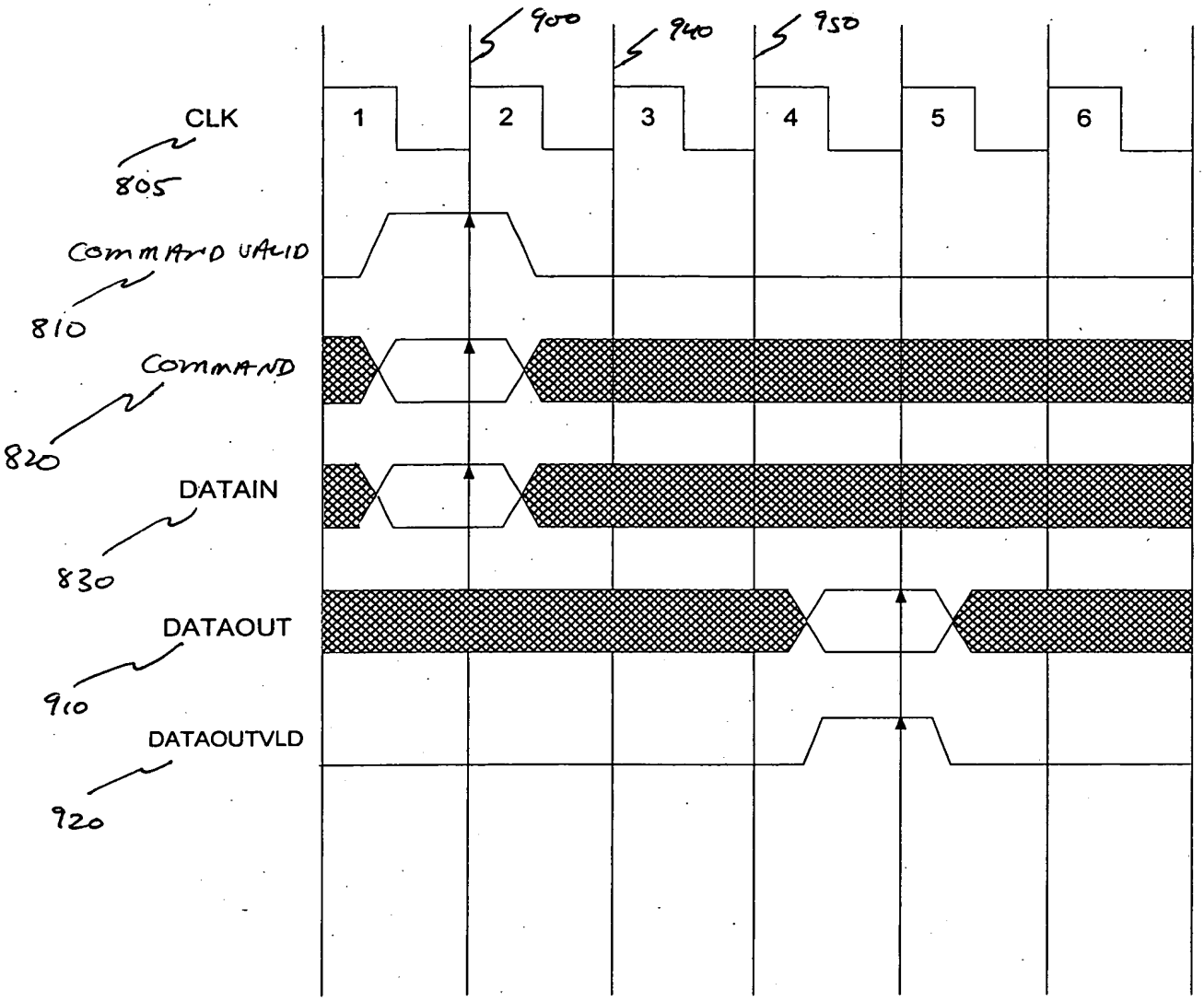

700
PRODUCT SPECIFICATION
Analog
Digital
730
DESIGN AT LEAST SOME ANALOG CIRCUITS
ROUGH DRAFT OF LOGIC
710
740
ESTIMATE NO. OF GATES
LAYOUT COMPONENTS FOR ALL ANALOG CIRCUITS
750
DESIGN EMULATOR
720
Analog
Digital
AFFIX ON CHIP
760
TEST
770
780
DOES ANALOG PORTION HAVE ACCEPTABLE RESPONSE?
NO
DESIGN/ REDESIGN AT LEAST SOME ANALOG CIRCUITS
785
yes
790
CAN LOGIC BE DESIGNED ACCORDING TO TEST RESULTS
No
yes/ digital
793
COMPLETE DIGITAL DESIGN
796
TEST OK?
yes
No
yes/analog
REWIRE EMULATOR FOR FINAL DESIGN;
798

Fig. 7



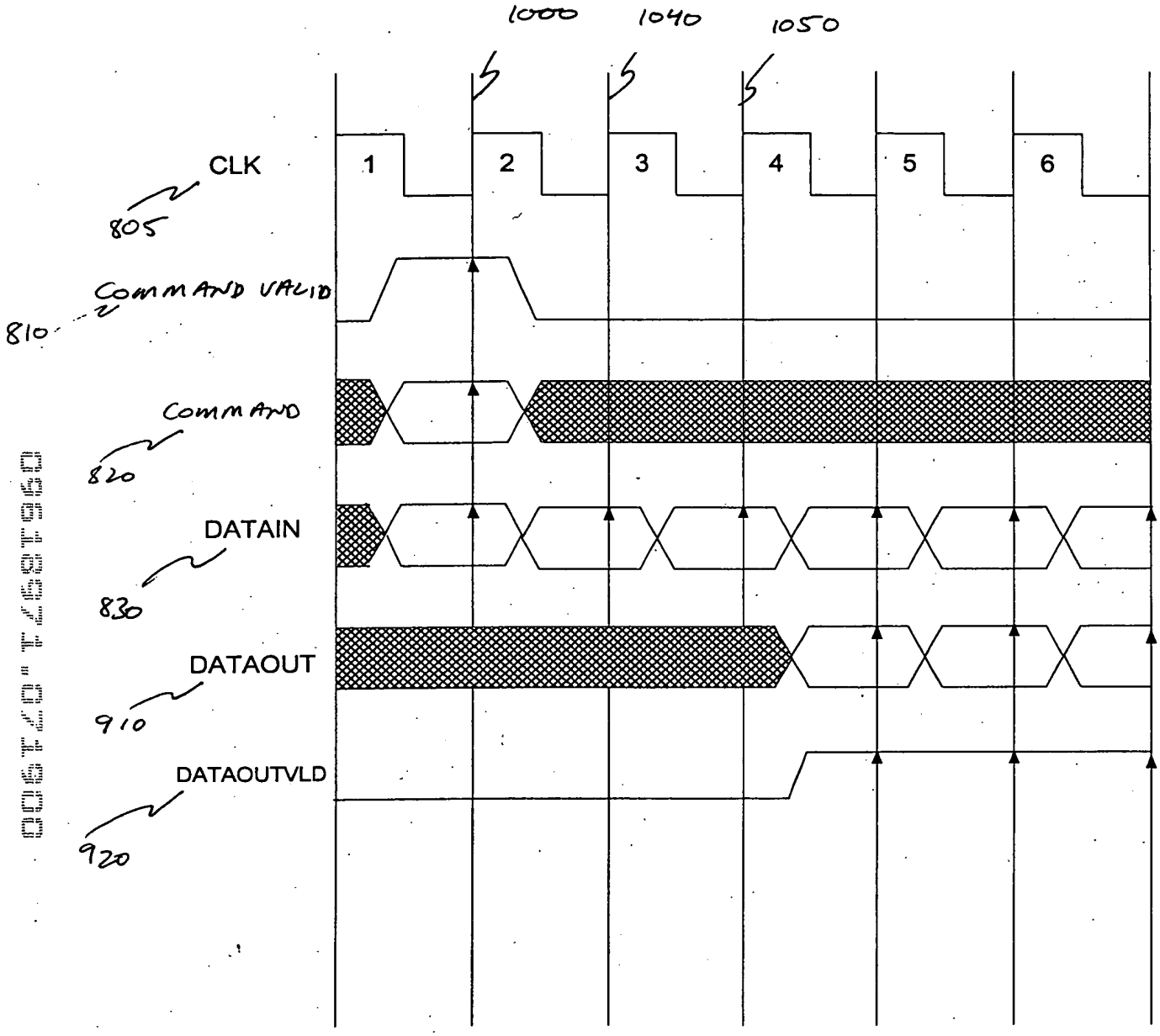

Configuration Register Write

fig. 8



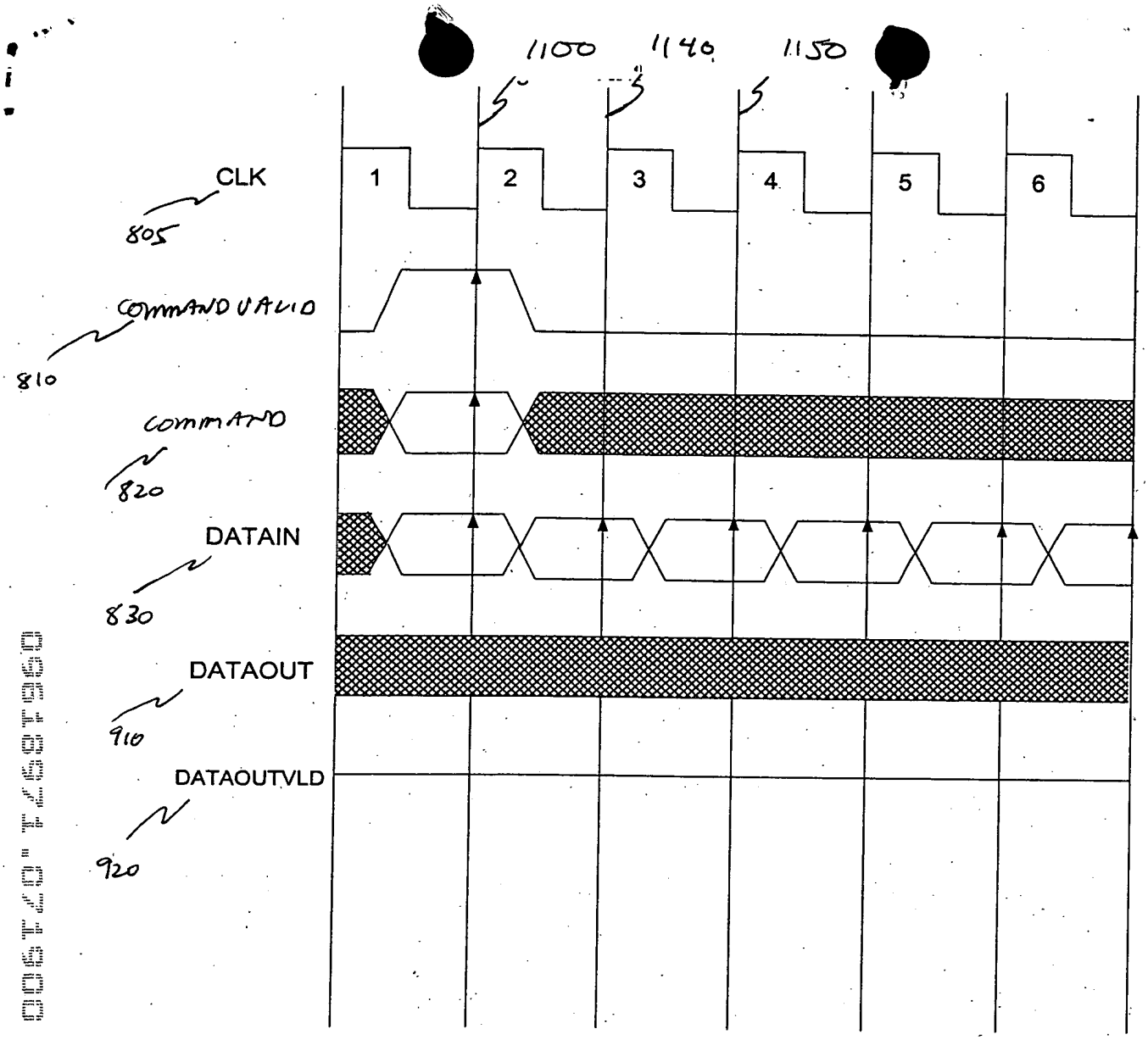

Configuration Register Read

Fig. 9




SHIFT TIMING

Fig. 10




Direct In

Fig. 11